IN THE CLAIMS

1.-11.(Canceled)

12. (Currently Amended) A new computer core having an interface to communicate with other cores, wherein the interface contains a plurality of interface signal carriers that are configurable, at compilation, such that at least [[of]] one of the interface signal carriers is selectively physically present in the interface or not physically present, wherein not physically present means that a route connection is not generated for an interface signal carrier selected to be not physically present.

13. (Previously presented) The computer core as set forth in claim 12, wherein the computer core is a core on a system on a chip and the other cores also belong to that system on a chip.

14. (Previously presented) The computer core as set forth in claim 12, wherein a first interface signal carrier is further configured to support different levels of functionality for the interface.

15. (Previously presented) The computer core as set forth in claim 14, wherein a signal carrier width of the first interface signal carrier is also configurable to support different signal widths.

16. (Currently Amended) A core on a system on a chip having an interface, wherein the interface contains a plurality of interface signal carriers that are configurable, at compilation, such that [[at least one of]] a first interface signal carrier[[s]] of the plurality of interface signal carriers is configurable to support different levels of functionality for the interface.

17. (Previously presented) The core as set forth in claim 16, wherein a signal carrier width of the first interface signal carrier is also configurable to support different signal widths.

18. (Currently Amended) The core as set forth in claim 16, wherein [[a]] the first interface signal carrier is configurable, at compilation, such that the first interface signal carrier is selectively physically present in the interface or not physically present.

19. (Previously presented) A method for generating at compilation a core interface for a system on a chip to enable re-use of the core with a different interface configuration, the method comprising:

providing configurable source code representative of the core interface for the system on a chip and identifying parameters of the core interface;

defining configuration parameters of the core interface; and

generating the core interface for the system on a chip from the configurable source code representative of the core interface and the identified parameters of the core interface configurable in accordance with the defined configuration parameters of the core interface.

20. (Currently Amended) The method as set forth in claim 19, wherein at least one of the configuration parameters of the core interface is defining whether a first interface signal carrier will be physically present in the core interface or not physically present.

21. (Previously presented) The method as set forth in claim 19, wherein at least one of the configuration parameters of the core interface is defining different levels of functionality that the core interface supports through a plurality of signal interface carriers.

22. (Previously presented) The method as set forth in claim 19, wherein at least one of the configuration parameters of the core interface is defining a signal width of a first interface signal carrier.